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Original Article

Design of a low noise single-ended sensor interface amplifier for bio-potential applications

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Keywords:
Chopping technique, flicker noise, low noise, low power, offset, sub-threshold

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Abstract
This paper discusses a low-noise read-out amplifier circuit for a biomedical sensor interface. The amplifier has two amplification stages with a Miller compensation capacitor that offers high gain with a large output swing. For power efficiency, all transistors are operated in a sub-threshold regime that makes the design suitable for implantable and portable medical devices. The proposed design works at the heart of bio-medical sensor interface circuits. It offersan amplification for different bio-potential signals such as electroencephalogram (EEG), electrocardiogram (ECG), and electromyogram (EMG) according to its bandwidth (BW). Furthermore, a small signal model analysis of the proposed amplifier is presented. A chopping technique is also proposed to reduce the sensor offset voltage and the flicker noise generated from sensor interface circuits. The proposed amplifier design achieves a gain and a BW of 62.16 dB and 506 Hz respectively. The input common-mode range (ICMR) varies from 0.3 V to 0.8 V with a phase margin (PM) of 62.57◦ at VCM equals 0.3 V and 66.8◦ at VCM of 0.8 V. The circuit is designed in 130 nm CMOS technology and consumes a power of 0.4 µW from 1 V supply. Also, the chopping technique reduces input-referred voltage noise from 38.445 µV/sqrt(Hz) to 3.06 µV/sqrt(Hz) within a frequency range from 0.01Hz to 500Hz.

1. INTRODUCTION

The Op-amp is considered the main building block in any analog integrated circuit. It is commonly used at the front end of bio-medical sensor interface circuits[1]. The main role of the amplifier is to amplify the sensed bio-potential signal from the human body to reach a suitable full-scale (FS) level for further signal processing, especially at the low-power analog to digital converter (ADC) input such as successive approximation register (SAR) ADCs[2,3]. For instance, the most famous bio-potential signals that originate from the human body are: ECG which comes from the Heart activity, EMG arises from the muscles activity, and EEG which results from the activity of the Brain[4]. The graphical abstract, depicted in Figure 1, illustrates the process of extracting bio-potential signals from various sources such as the brain, muscles, or heart activity using an electrode interface circuit. The bio-potential signal captured by the electrode is subsequently amplified to an appropriate level for further processing in the digital domain. The characteristics of the most famousbio-potential signals are illustrated in more detail as shown in Table 1. As presented, most of these signal amplitudes range from 0.001 - 5 mV and BW from 0.5-500 Hz. Consequently, a lot of design challenges arise when acquiring and amplifying these signals as they all originated from a noisy environment within the human body.

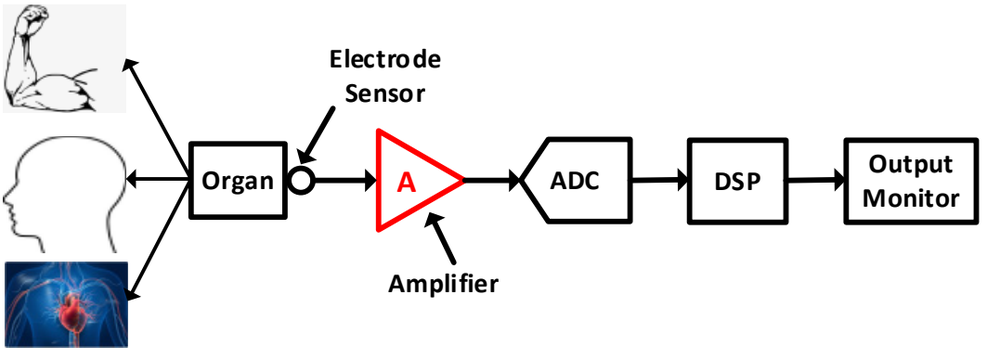

Fig. 1: Block diagram of biomedical system

Table 1: Characteristics of bio-potential signals[4].

Bio-Potential Signals	Amplitude(mV)	Frequency Range (Hz)
EEG	0.001 to 0.3	0.5 to 100
ECG	0.5 to 4	0.01 to 250
EMG	0.1 to 5	Up to 500

For signal amplification, there are many types of operational trans-conductance amplifier topologies such as folded cascode, telescopic cascode, single OTA, and two-stage amplifiers. Table 2 illustrates the comparison between these four types in terms of their specifications (DC gain, output swing, CMIR, efficiency, noise, and stability). From Table 2 it can be seen that the two-stage amplifier topology is the best candidate for higher DC voltage gain, larger output swing, and large ICMR, however, this comes with a trade-off with high power dissipation, high Noise, and poor stability. The higher noise, in this case, is mainly because of flicker noise which is a real problem, especially in biomedical applications as it represents the dominant noise source at lower frequencies.There are several techniques available for reducing noise and DC-offset in electronic circuits. One such technique is Correlated Double Sampling (CDS), which is particularly effective in data acquisition systems. CDS minimizes offset errors and reduces noise by subtracting an initial reference sample from subsequent samples. Another technique commonly used for low-frequency noise reduction is Auto-zeroing (AZ). AZ involves periodically measuring and canceling the offset error to improve circuit accuracy. Additionally, the chopping technique is employed to shift noise and offset to higher frequencies. It involves modulating the input signal and using synchronous demodulation to extract the desired signal while rejecting noise.

By utilizing techniques such as CDS, AZ, and chopping, along with appropriate stability enhancement methods, electronic circuits can achieve enhanced performance and reliability. These techniques are especially valuable in biomedical applications where accurate signal acquisition and processing are crucial.In addition to noise and offset reduction, stability enhancement is crucial in electronic circuits. One method for stability enhancement is the use of a Miller compensation capacitor. This capacitor helps in improving the stability of amplifiers and reducing the risk of instability. Additionally, in certain cases, adding a resistor in conjunction with the Miller compensation capacitor can further enhance stability and reduce power dissipation associated with stability improvement.

Accordingly, this paper proposes different techniques to overcome the aforementioned problems. In this work, all the circuit transistors are designed in the sub-threshold region to achieve higher power efficiency. In addition, the chopping technique is used to overcome the flicker noise and DC offset problems. Furthermore, Miller compensation capacitance is used to get an unconditionally stable design. These solutions are introduced in more detail throughout the paper.

This paper is organized as follows. Section II presents the two-stage amplifier design with Miller capacitance. Section III discusses the chopper circuit integration with the single-ended amplifier design. Section IV provides the simulation results of the proposed amplifier circuit. Finally, Section V concludes the paper.

Table 2: OTAs comparison

spec	Miller	Telescopic	Folded	5T OTA
DC gain	V.Good	Good	typical	Bad
O/P swing	V.Good	Bad	typical	good
CMIR	Good	bad	V.Good	typical
Efficiency	Bad	Good	sufficient	V.Good
Noise	Bad	Good	sufficient	V.Good
Stability	Bad	Good	sufficient	V.Good

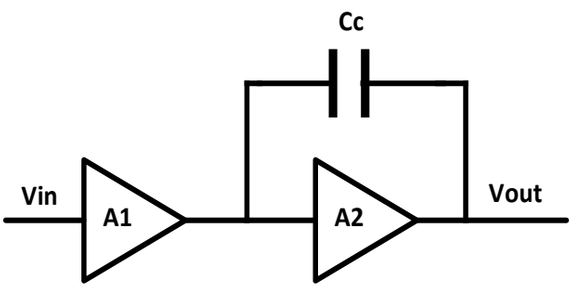

Fig. 2: Block Diagram of Two Stage Amplifier with Miller capacitor

2. TWO-STAGE AMPLIFIER DESIGN WITH MILLER CAPACITANCE AND RESISTANCE

The top-level block diagram of the two-stage amplifier with Miller compensation capacitor is illustrated in Figure 2. It consists of two amplification stages and a compensation capacitor CC The first stage (A1) is represented by an operational Trans-conductance Amplifier (OTA) that contributesmost of the amplifier gain while the second stage (A2) achieves a large output swing

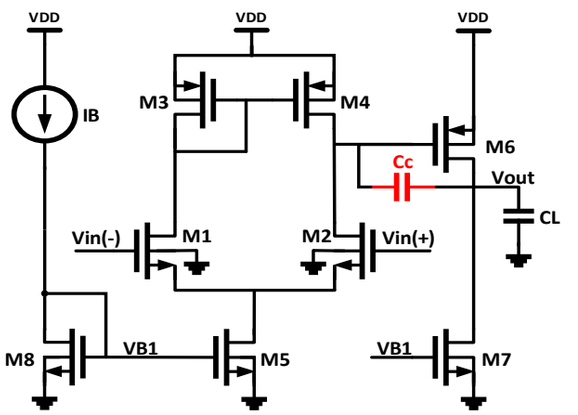

Fig. 3: Schematic of CMOS single-ended Two Stage Amplifier with Miller compensation capacitor.

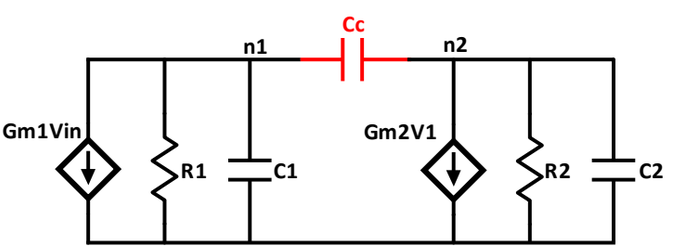

Fig. 4: Small Signal Model of the Two-Stage Amplifier using only compensation capacitance.

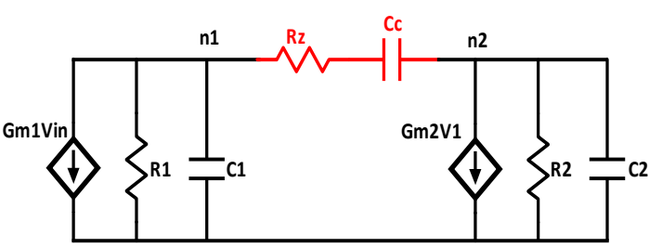

Fig. 5: Small Signal Model of the Two-Stage Amplifier using compensation capacitance and resistance.

The Miller compensation capacitor is inserted in a parallel path between the second stage's input and the output terminal. Figure 3 shows a detailed circuit schematic of a single-ended two-stage differential amplifier with a Miller compensation capacitor. The first OTA stage consists of transistors from M1 to M5. The first two transistors M1 and M2 work as differential input pairs. Whereas M3, which is connected as a diode-connected Transistor, and M4 represent the OTA load. To bias the first OTA stage, M5 works as a current source. The output from the OTA, which is the drain of M4, is connected to the gate of M6 which represents the input of the second stage. On the other hand, the second stage is represented as a common source amplifier with a current source load of M7. The compensation capacitor CC is connected between the gate of M6 and its drain which is also connected to a capacitive load CL[5]. From Miller's approximation, a large capacitance can be seen when looking at the input terminal of the second stage. Also, almost the same capacitance is seen locking from the output of the second stage. Miller approximation capacitance significantly affects the design stability as the large capacitance pushes the dominant pole to the left-hand side and the lower capacitance at output approximately maintains the first non-dominant pole at the same value. Accordingly, a good separation between the dominant and first non-dominant pole is maintained which results in increasing phase margin (PM) and thus the stability enhancement of the proposed amplifier. In addition to stability enhancement, miller capacitance reduces the DC offset voltage of the proposed circuit[6]. As the design targets ultra-low power consumption, to be suitable for implantable and portable biomedical devices, all amplifier transistors are designed to operate in a sub-threshold regime. Accordingly, high power efficiency is maintained.

To have an accurate model for the sub-threshold region transistor, let's start with the saturation region model and adapt it accordingly to the sub-threshold case. The equivalent small-signal model for a single transistor working in a sub-threshold region is the same as that of the saturation region, however, the trans-conductance (gm) and output resistance (ro) will be significantly different[7,8]. The sub-threshold trans-conductance gm is represented as:

$$g_m = \frac{I_{sub}}{n_n \cdot V_T} \quad (1)$$

Where I_{sub} is the transistor sub-threshold current, n_n is the sub-threshold coefficient, and V_T is a thermal voltage which is given by,

$$V_T = \frac{K \cdot T}{q} \quad (2)$$

Where K is the Boltzmann constant, T is the temperature in Kelvin, and q is the electron charge. While n_n is represented as,

$$n_n = 1 + \frac{C_{dep}}{C_{ox}} \quad (3)$$

Where C_{dep} is the depletion-layer capacitance per unit area, C_{ox} is the gate capacitance per unit area.

$$I_{sub} = I_O \cdot e^{\left(\frac{V_{GS}-V_{th}}{n_n V_T}\right)} \cdot \left(1 - e^{\frac{V_{DS}}{V_T}}\right) \quad (4)$$

Where V_{th} is the sub-threshold voltage. I_O is given by:

$$I_O = \mu C_{ox} \left(\frac{W}{L}\right)(n_n - 1)V_{th}^2 \quad (5)$$

Where V_{th} is the threshold voltage. The transistor output resistance is given by,

$$r_o = \frac{1}{\eta * g_m} \quad (6)$$

Where η is the drain-induced barrier-lowering coefficient.

Figure 4 depicts a small-signal model of the proposed design of the two-stage amplifier with Miller compensation working in the sub-threshold regime. Detailed circuit analysis is performed throughout the proposed work to have an accurate small-signal model for the proposed design. By applying and solving KCL equations at nodes n1 and n2, the following transfer function is obtained[9],

$$\frac{V_{out}}{V_{in}} = \frac{G_{m1} G_{m2} R_1 R_2 \left(1 - \frac{SC_c}{G_{m2}}\right)}{a \cdot S^2 + b \cdot S + 1} \quad (7)$$

Where:

$a = R_1 R_2 (C_1 C_2 + (C_2 + C_1) C_C)$

$b = (R_1 (C_1 + C_C) + R_2 (C_2 + C_C) + R_1 R_2 G_{m1} C_C)$

Gm1 is the trans-conductance of the first amplifier stage, and Gm2is the trans-conductance of the second stage. Also, R1 and R2 are the total output resistances of the first and second amplifier stage and equal to $\backsimeq r_{O2} // r_{O4}$, and $\backsimeq r_{O6} // r_{O7}$ respectively. The transfer function formula for a second-order system with zero feedthrough is equal

$$\frac{V_{out}}{V_{in}} = \frac{A_O \left(1 - \frac{S}{\omega_z}\right)}{S^2 \left(\frac{1}{\omega_{P1}\omega_{P2}}\right) + S\left(\frac{1}{\omega_{P1}} + \frac{1}{\omega_{P2}}\right) + 1} \quad (8)$$

Comparing equations 7 and 8 while making some approximations and reductions, the following formulas can be obtained,

$$\omega_{P1} = \frac{1}{R_1 (G_{m2} R_2) C_C} \quad (9)$$

Where ωP1 represents the dominant pole, while the non-dominant pole can be written as

$$\omega_{P2} = \frac{G_{m2}}{C_2} \quad (10)$$

The zero feed through due to Cc is derived as:

$$\omega_Z = \frac{G_{m2}}{C_C} \quad (11)$$

Also, the gain bandwidth product equals

$$GBW = \frac{G_{m1}}{C_C} \quad (12)$$

And finally, the DC voltage gain of the amplifier is

$$A_{DC} = G_{m1} G_{m2} R_1 R_2 \quad (13)$$

From the derived equations, the zero feed-through of CC needs to be larger than GBW to reduce its effect on the amplifier stability. As a result, Gm2 is selected to be 10 times larger than *Gm1* (*Gm2* = 10*Gm1*)[5]. Consequently, the PM is then can be expressed as,

$$PM = 84.29 - \arctan\left(\frac{C_2}{10C_C}\right) \quad (14)$$

To further enhance the amplifier stability and reduce power dissipation, another compensation type is presented. Resistance in series with CC compensation capacitor is used. Figure 5 shows an equivalent small-signal model for the proposed design with added compensation resistance. By following the previous steps, a new equation describes the zero feed-throughs can be obtained as follows[10];

$$\omega_Z = \frac{1}{\left(\frac{1}{G_{m2}} - R_z\right)C_C} \quad (15)$$

Resistance R_z is implemented using a transmission gate to make it almost has a constant value with the input signal. Choosing $R_z > \frac{1}{G_{m2}}$ shifts the left-hand side zero more to the left which reduces the effect of the zero on stability and increases the stability margin. The extra PM achieved from using R_z can be traded off to reduce the power consumption of the proposed design. R_z can be implemented within the amplifier using a transmission gate as it will be shown in the next section.

Table 3: selected length and W/L ratio for our design

W/L ratio	length (L)	MOSFET
30	300 nm	M1,M2
25	280 nm	M3,M4
2	2um	M5,M8
240	300nm	M6
11.5	2um	M7

Target design specifications have been achieved throughout the proposed design based on the derived formulas. The amplifier design is done and simulated using the Cadence Virtuoso design environment. Accordingly, Table 3 shows the length and W/L ratio for each transistor in the amplifier circuit. According to the design equations, the Miller compensation capacitor is chosen to be (Cc) = 135 fF. The proposed amplifier circuit achieves a range of specifications based on the common-mode input voltage (VCIM). For instance, it achieves a gain and a bandwidth of 62.16 dB and 561 Hz respectively. The achieved BW covers the frequency range of all bio-Potential signals. The circuit consumes 400 nW of power from a 1 V supply. The input common-mode range (ICMR) varies from 0.3 V to 0.8 V with a phase margin (PM) of 62.57◦ at VCM equals 0.3 V and 66.8◦ at VCM of 0.3 V. The input-referred noise is 38.4455 uV/sqrt(Hz) across the frequency range from 0.01 Hz to 500 Hz. This value is considerably large during bio-Potential signals acquisition. The large value of noise concentrates at a very low frequency as it comes from MOSFETs flicker or 1/f noise.

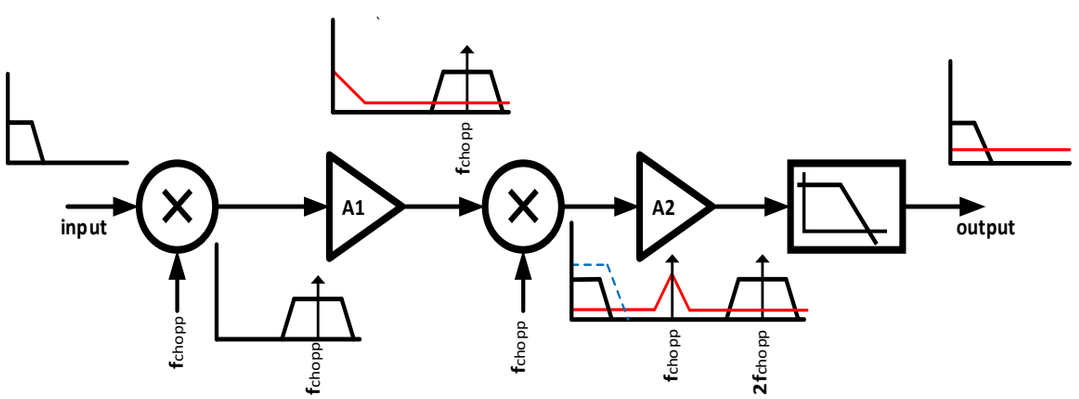

Fig. 6: Block Diagram of chopper circuit

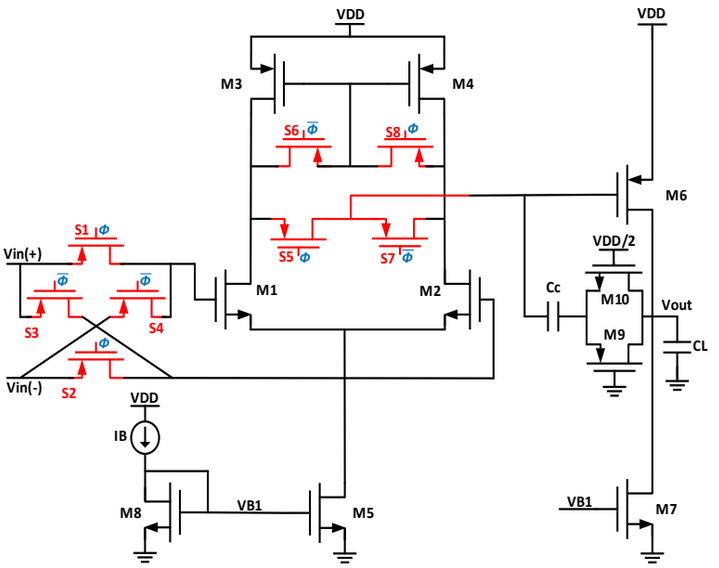

Fig. 7: Schematic of the two-stage differential amplifier with chopper technique

3 CHOPPER CIRCUIT IN A SINGLE-ENDED COMPENSATED TWO-STAGE AMPLIFIER

Across bio-potential signals, BW, flicker noise, and DC offset are the most important sources of acquisition errors. To reduce the effect of offset and flicker noise in CMOS amplifiers, the Chopping technique is proposed[11, 1]. For a single CMOS transistor, the flicker noise power equals,

$$V_n^2(f) = \frac{K}{C_{OX}WL} * \frac{1}{f} \qquad (16)$$

Where K is the flicker noise coefficient, W is the transistor width, L is the channel length, and COX is the gate oxide capacitance per unit area. The chopping technique is an analog modulation technique that can be applied within the circuit to tackle the offset and flicker noise problems. This can be done using two steps of modulation/demodulation. First, the input bio-potential signal is applied to the first chopper circuit as shown in Figure 6. Consequently, the signal is modulated and shifted to the higher frequency of f_{chopp}. Next, the modulated signal is amplified along with the amplifier input-referred flicker noise by the gain of the amplifier. Second, another chopper circuit demodulates the amplified bio-potential signal back to the baseband and meanwhile modulates the flicker noise to the higher frequency of f_{chopp} and its harmonics. A low pass filter is then used to filter out any f_{chopp} harmonics while passes only amplified input signal without any flicker noise and offset as depicted in Figure 6.While the chopping technique is effective in reducing low-frequency noise and DC-offset, it introduces certain overheads in terms of power consumption and circuit area. These overheads arise from the digital circuitry required to generate the necessary non-overlapping clocks for modulation and demodulation processes. Despite these overheads, the chopping technique remains a valuable approach for reducing low-frequency noise and offset. However, designers must carefully evaluate the trade-offs between noise reduction benefits and the associated power consumption and circuit area requirements. Figure 7 shows the transistor level schematic of the two-stage amplifier with the chopper circuit where ϕ and $\bar{\phi}$ represents a non-overlapping clock from f_{chopp} in Figure 6. The chopper circuit itself consists of four transistors S1 − S4 that switch ON and OFF according to the applied clock phase. When the clock is high then S1 and S2 are switched ON and S3 and S4 are switched OFF and the input signal is applied directly to the amplifier input. On the other hand, when the clock is low, S1, S2 are turned off and S3, S4 are turned ON and the input signal polarity is alternated before it appears at the amplifier input. The chopping signals ϕ and $\bar{\phi}$ are designed as non-overlapping clocks. The second modulation/demodulation circuit is constructed from transistors S5 − S8. It works with the same theory as the first chopper stage; however, it modulates the flicker noise while demodulating the input bio-potential signal[12]. The chopper circuit used in the proposed single-ended two-stage amplifier reduces the flicker noise generated from the first amplifier stage, however, the noise from the second stage is not affected. Rz is implemented using a transmission gate which is constructed by M9 and M10 as shown in Figure 7. To maintain fast settling, the chopper transistor switches ON resistance Ron is reduced. It is noted that all N-MOSFET bodies are connected to the ground and the P-MOSFET bodiesare connected to VDD for the whole design. Accordingly, the width and length of the designed chopper transistors are presented as shown in Table 4,

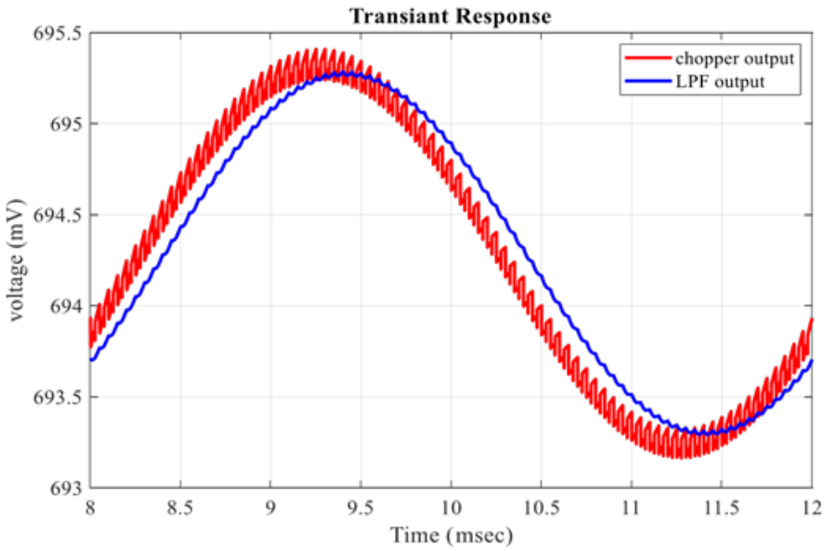

Fig. 8: Transient response of two-stage amplifier with chopper circuit

Table 4: Designed Width and Length of chopper circuit transistor

MOSFET	Length (L)	Width (W)
S1 − S4	120 nm	5 um
S5 − S8	120 nm	160 nm

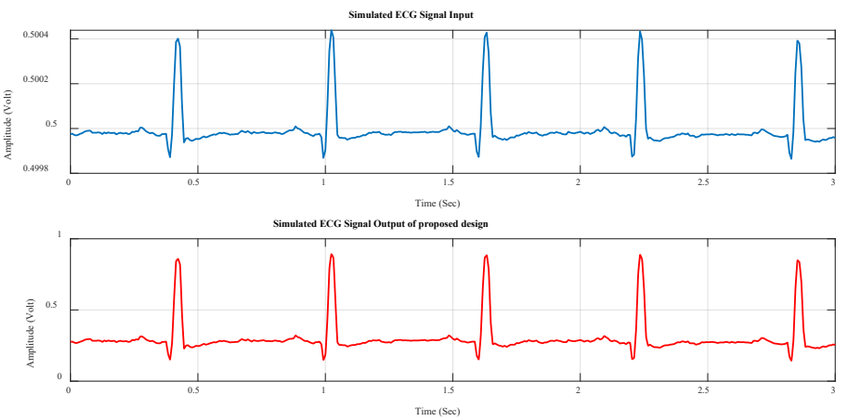

Fig. 9: Transient response of ECG signal at $V_{CM} = 0.5V$

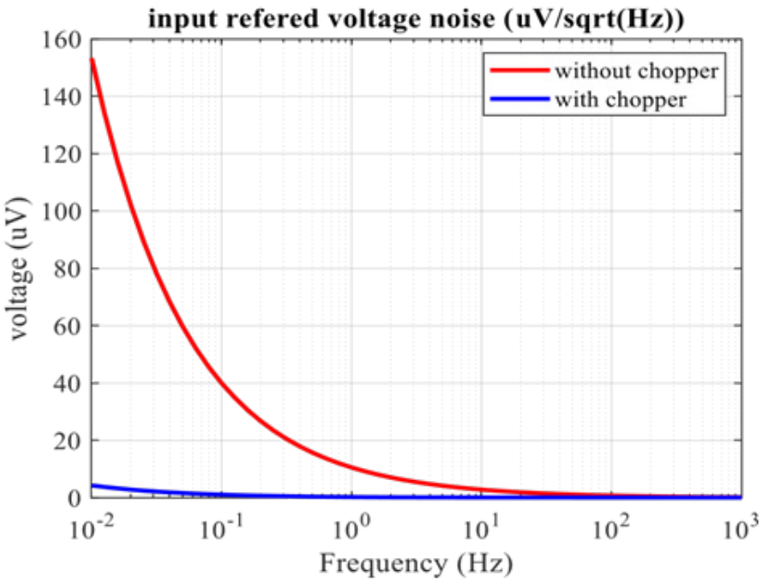

Fig. 10: Simulated input referred voltage noise for the two-stage amplifier with Miller capacitance and other with additional chopper circuit

4. SIMULATION RESULT

The designed circuit is simulated in a Cadence Virtuoso analog environment using UMC 130 nmCMOS technology with a high-speed low threshold voltage transistor model. The transient response of the proposed circuit with the chopper circuit as a response to a sinusoidal signal is illustrated in Figure 8. As shown, after the chopping is applied, the output signal from the amplifier is spiked due to the harmonic frequency components of the chopper frequency. To get rid of these spikes and higher-order harmonics pass only the signal of interest, a low-pass filter (LPF) is used. To mimic the real amplification of bio-potential signals, the proposed circuit is also simulated with a real ECG signal.

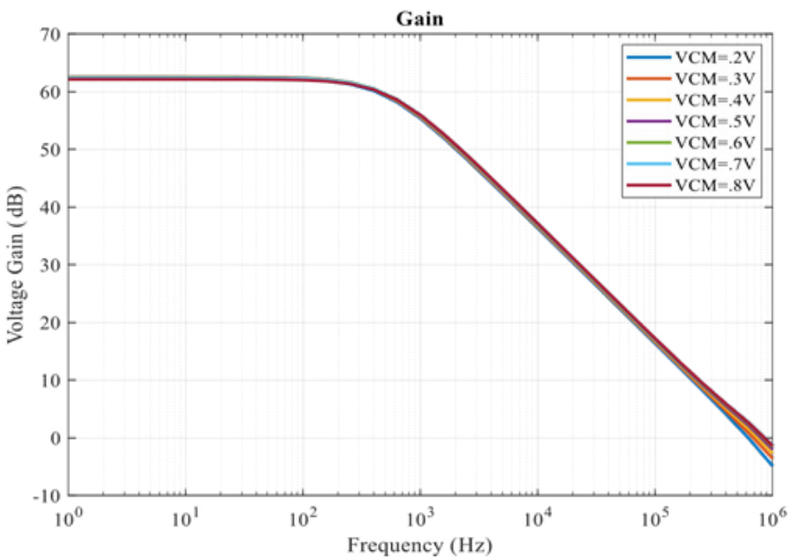

Fig. 11: Simulated voltage gain at common mode voltage from 0.2V to 0.8V

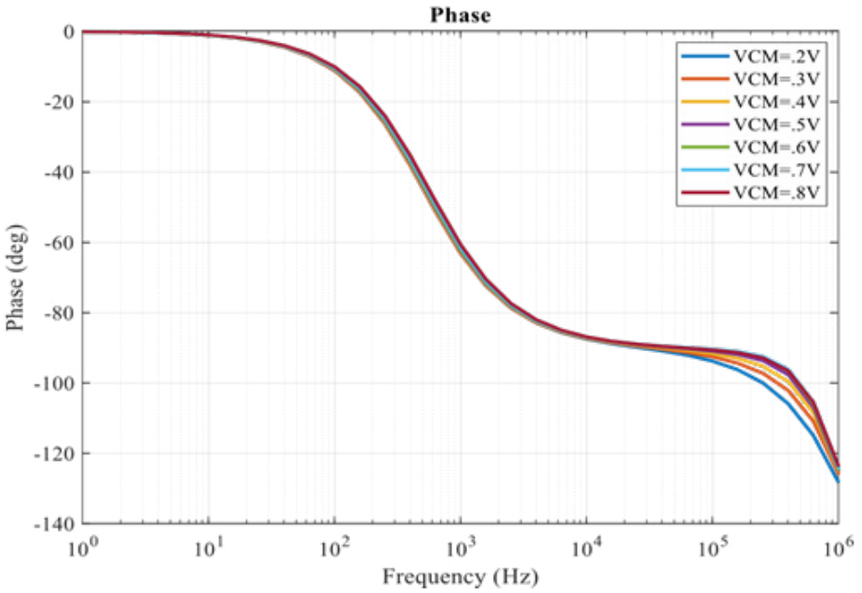

Fig. 12: Simulated phase at common mode voltage from 0.2V to 0.8V

As depicted in Figure 9, ECG signal is applied with 444 uV amplitude (upper curve) and it is amplified by 62 dB of gain at the proposed circuit output (lower curve). The chopping clock frequency fchopp equals 20 KHz is used in the proposed design. Using the chopper technique, the input-referred voltage noise is reduced from 38.4455 uV/sqrt(Hz) to 3.063 uV/sqrt(Hz) across the frequency range from 0.01 Hz to 500 Hz which is a considerable enhancement in the integrated noise as seen in Figure 10.

Figure 10 shows the amplifier voltage gain across frequency at different values of commonmode input voltage from 0.2 V to 0.8 V. Furthermore, Figure 12 shows the proposed amplifier phase response. From the gain and Phase response, it can be deduced that the phase margin (PM) varies from a minimum of 62.57◦ with 3dB bandwidth 566 Hz at VCM equals 0.8 V and a maximum of 66.15◦ with 3dB bandwidth521 Hz at VCM of 0.4 V. That ensures the amplifie stability for the entire common-mode range. The common-mode rejection ratio is presented in Figure 12 which has a value of 81.654 dB after applying the chopping technique. To test the circuit robustness, Figure 13 illustrates the voltage gain at process corners with a power supply variation of 1 V +/-10% and temperature variation from -40 ◦C to 85 ◦C. The circuit shows a DC voltage gain variation from 66 dB to 52 dB. The achieved design performance is listed in Table 5 which shows a comparison with other state-of-the-art designs. As shown in Table V, the proposed design achieves the lowest IRN across the BW of 0.01 HZ to 500 Hz which makes it suitable for bio-potential applications.

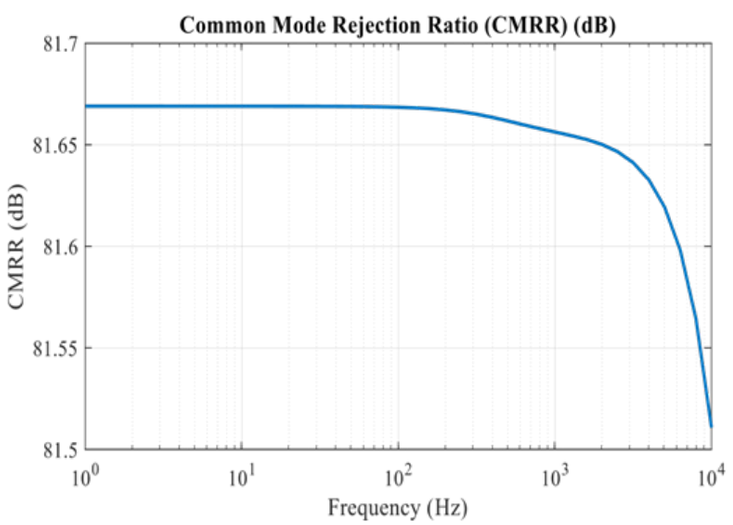

Fig. 13: Simulated CMRR for two-stage amplifiers with chopper circuit compensation capacitor and resistor at common mode voltage = 0.5V

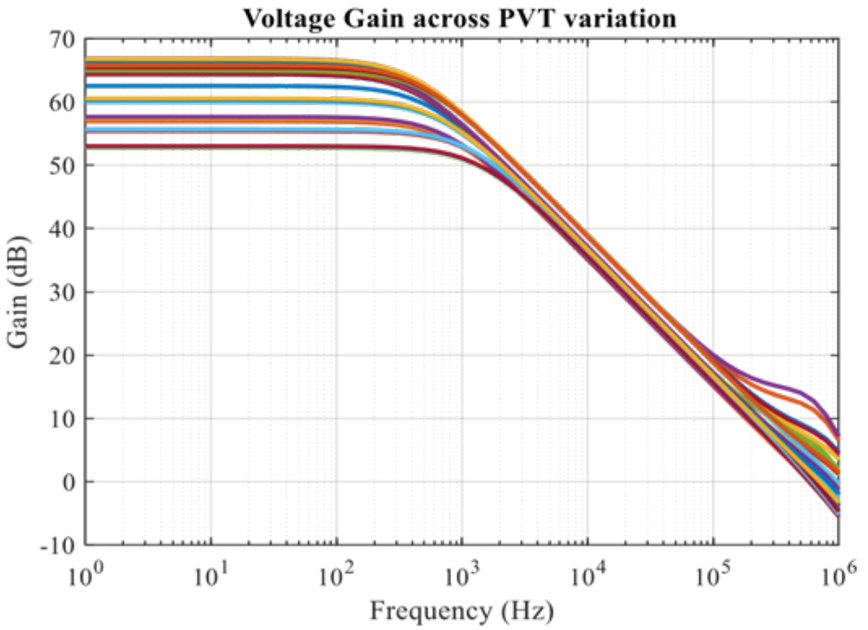

Fig. 14: Voltage Gain across Process Corners, 1V % 10 of Supply Voltage Variation and different temperature (PVT)

Table 5: Result parameter of our simulation with a comparison with other work

specification	This work	[13]	[14]	[15]	[16]	[17]	[18]	[19]
power supply (V)	1	1	1.8	0.6	0.6	1.8	0.85	1.8
DC Gain (dB)	62.16	55.2	45.38	86.7	39	40	62	34.7
PM	62.57	69.46	NA	61.5	NA	61	NA	NA
CMIR (V)	0.6 V	NA	NA	NA	NA	NA	NA	NA
technology nm	130	90	180	45	180	180	45	180
IRN (uv/sqrt(Hz))	3.06[1]	0.138[2]	1.62[3]	1820	2.3	0.031[4]	3.83[5]	0.25[6]
power dissipation (uW)	0.4	2.6	6.25	12	0.69	8	1.5	4.2
load capacitance (pF)	1	1	NA	NA	NA	10	NA	NA
Bandwidth *KHz*	0.505	15.3	2.9	227	0.173	1	0.1	0.1
CMRR dB	81.65	131	NA	129	74	84	176	71.5

[1]IRN over bandwidth from .01 Hz to 500 Hz. [2]IRN at 10 Hz. [3]IRN at 1 Hz.[4]IRN at 1000 Hz. [5]IRN at 10Hz [6]IRN at 100 kHz

5. CONCLUSION

In this paper, a single-ended two-stage differential amplifier with a miller compensation capacitor and resistor is designed. A High gain amplification with a bandwidth up to 505 Hz (which is sufficient for EEG, ECG, and EMG) has been achieved at a low power dissipation of 400 nW. Regarding stability, a good phase margin of 63 deg is achieved. Furthermore, a sub-threshold transistor model for low-power operation is introduced. Also, a chopper technique is introduced to reduce the amplifier's input refereed noise from 38.445 uv/sqrt(Hz) to 3.064 uv/sqrt(Hz) across the bandwidth from 0.01 Hz to 500 Hz.

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